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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/821,095	03/30/2001	Koichi Hashimoto	740250-837	2229

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EXAMINER	
POPOVICI, DOV	
ART UNIT	**PAPER NUMBER**
2625	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/20/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	09/821,095	HASHIMOTO ET AL.	
	Examiner	Art Unit	
	Dov Popovici	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☒ Claim(s) *2-5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Dov Popovici
DOV POPOVICI
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Iwata et al (U.S. 4,514,826) in view of Ibaraki et al (U.S. 5,617,476).

As to claim 1, Iwata et al discloses an image processing apparatus comprising: At least two signal processor modules (PE1, PE2, see Fig. 3) interconnected with each other in series, each of the signal processor modules (PE) having an input port through which data is input, a memory (M11, B12, M13) which stores data, a signal processor portion (P) which carries out processing on input data according to a program and an output port (see fig. 3) through which data is output. Iwata et al shows in fig. 3 that the processor P has two outputs, one is connected to PE2 and the other is connected to the bus.

Iwata does not specifically states that at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

Ibaraki et al teaches a separator 81 in fig. 8 A, that outputs both processed data and unprocessed data in parallel (see fig. 8A).

Therefore, it would have been obvious to one of ordinary skilled in the art to have modified Iwata et al wherein: the at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

The motivation for doing so would be to increase the speed of processing data in the second processor in a series of processors, whereby, the unprocessed data does not have to pass through the second processor in a series processing, so that the unprocessed data can be forward directly to the output port, while less data is passing through the subsequent processing module.

Allowable Subject Matter

Claims 2-5 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record (namely, Iwata et al (U.S. 4,514,826) and Ibaraki et al (U.S. 5,617,476) do not disclose, teach or suggest, processor stores within one cycle in the memory unprocessed data as input and processed data obtained by reading out and processing unprocessed data stored in the memory predetermined number of cycles before and outputs within one cycle through the output port unprocessed and processed data stored in the memory predetermined number of cycles before, and the

other processor stores within one cycle in the memory unprocessed as input and processed data obtained by reading out and processing unprocessed data stored in the memory predetermined number of cycles before and outputs within one cycle and outputs through the output port unprocessed input data stored in the memory predetermined number of cycles before, as claimed in claim 2.

The prior art of record (namely, Iwata et al (U.S. 4,514,826) and Ibaraki et al (U.S. 5,617,476) do not disclose, teach or suggest, a mounting means on which a signal processor module is removably mounted, provided for at least one of the processor modules; and a switching means is provided for said at least one processor module to transfer data to the processor module through its input port when it is mounted on the mounting means and to transfer the same to a component forward of the processor module when it is not mounted on the mounting means, as claimed in claim 5.

Response to Arguments

Applicant's arguments filed 10/10/2006 have been fully considered but they are not persuasive.

Applicant argues that "there is teaching, disclosure or suggestion of any image processing apparatus or capability in the relational algebra engine for using in a relational database system of Iwata" and "It is clearly disclosed that fig. 3 of Iwata is a block diagram of a relational algebra engine for performing sort/merge algorithm, which is clearly and completely unrelated to imaging processing and the signal processor modules utilized in image processing in Applicant's claimed invention", and "Should the

examiner continues asserting that Iwata teaches an image processing system and signal processors, Applicants would respectfully request the examiner to provide support by pointing out where in Iwata such disclosure can be found.", the arguments have been fully considered but they are not found to be persuasive because the of following reason(s):

(1) In response to applicant's arguments, the recitation "An image processing apparatus" has not been given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

(2) Iwata et al discloses at least two signal processor modules (PE1, PE2, see Fig. 3) interconnected with each other in series, each of the signal processor modules (PE) having an input port through which data is input, a memory (M11, B12, M13) which stores data, a signal processor portion (P) which carries out processing on input data according to a program and an output port (see fig. 3) through which data is output. Iwata et al shows in fig. 3 that the processor P has two outputs, one is connected to PE2 and the other is connected to the bus.

Applicant argues that "Ibaraki does not teach, disclose or suggest at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data, as recited in Applicants' claim 1." And that "examiner erroneously equated the separator 81 to Applicants' signal processor modules" and that "separator 81 of Ibaraki is not a signal processor module and does not have its own memory and signal processor portion", the arguments have been fully considered but they are not found to be persuasive because the of following reason(s):

(1) In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(2) Iwata et al. is cited to teach at least two signal processor modules (PE1, PE2, see Fig. 3) interconnected with each other in series, each of the signal processor modules (PE) having an input port through which data is input, a memory (M11, B12, M13) which stores data, a signal processor portion (P) which carries out processing on input data according to a program and an output port (see fig. 3) through which data is output. Iwata et al shows in fig. 3 that the processor P has two outputs, one is connected to PE2 and the other is connected to the bus.

Iwata et al. does not specifically states that at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

Ibaraki et al. is cited by the examiner to teach a separator 81 in fig. 8 A, that outputs both processed data and unprocessed data in parallel (see fig. 8A).

Therefore, it would have been obvious to one of ordinary skilled in the art to have modified Iwata et al. wherein: the at least one of the signal processor modules outputs in parallel both unprocessed input data and processed data obtained by processing the input data.

The motivation for doing so would be to increase the speed of processing data in the second processor in a series of processors, whereby, the unprocessed data does not have to pass through the second processor in a series processing, so that the unprocessed data can be forward directly to the output port, while less data is passing through the subsequent processing module.

Applicant argues that "Applicants would respectfully request the examiner to at least provide the rationale for combining a relational algebra engine for use in a relational database of Iwata with an audio scrambling system of Ibaraki" the arguments have been fully considered but they are not found to be persuasive because the of following reason(s):

(1) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by

combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine in the rejection is found in the knowledge generally available to one of ordinary skill in the art.

(2) The motivation for doing so would be to increase the speed of processing data in the second processor in a series of processors, whereby, the unprocessed data does not have to pass through the second processor in a series processing, so that the unprocessed data can be forward directly to the output port, while less data is passing through the subsequent processing module.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dov Popovici whose telephone number is 571-272-4083. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Coles can be reached on 571-272-7402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dov Popovici
Primary Examiner
Art Unit 2625